High Tree
IST–2001-38931
High-Speed Three-Dimensional Chip-to-Chip Communication

Final Report

Covering period 1 January 2003 to 30 June 2005

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Project Co-ordinator:	ARCES University of Bologna
Partners:	STMicroelectronics, CEA-LETI

Project funded by the European Community under the "Information Society Technologies" Programme (1998-2002).

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1. Executive Summary

To meet the demand of future electronic products with more functionality, reduced size, low cost and high performance in terms of speed and power consumption and to enable in one single die mix technologies (memories, logic, CMOS analog, RF, MEMs), the traditional System-on-chip approach has shown many issues.
The two dimensional planar assembly integration has reached its limits and the deep-submicron technology that makes possible the Giga-Scale integration does not help to solve the problems. The higher current gives rise to static and dynamic IR voltage drop issues and reliability degradation due to electro-migration. The smaller geometry and denser pattern lead to RC delay increase and signal integrity problems (crosstalk noise, delay fluctuation). The higher speed causes inductance related issues and electro-magnetic interference (EMI) problems.
Three-dimensional (3D) IC technology is emerging as a solution able to mitigate the interconnect crisis issue and it seems very promising for heterogeneous integration of systems.
Today, several 3D approaches allow to stack packaged chips, several emerging technologies shows 3D die stacking (packaged chips, stacked dies, System in package, Multi-chip module). There are also many 3D process options (Silicon Beam recrystallization, multiple stacks of wafer layers, solid phase crystallization) and many types of vertical connection (back and through vias, metal-stud/via, bumps) can be implemented. However the problems of the limited communication bandwidth between chips and high-power high-pin parallelism have not been solved. Researchers are looking at a variety of methods to increase the density of interconnection performances. The ***High Tree*** project aims at investigating interconnection techniques that improve the current situation in term of available pin count in 3D structures, communication bandwidth and dissipated power.
The goal is twofold:

1. The study and implementation of a 3D technology compatible with advanced CMOS process that is able to support high speed inter-chip communication bandwidth with reduced pin pitch and power dissipation.
2. The study and implementation of a 3D alignment methodology compatible with advanced CMOS technology

For the first objective, capacitive coupling interconnection has been proposed as a means to enable high data rate communication bandwidth. During this project, a set of cells suitable for data and clock communication have been proposed to demonstrate the feasibility of the wireless capacitive coupling principle. A prototype with clusters of different communication channels was integrated in 0.13um STM technology. In term of process development, two different approaches have been investigated to enable the implementation of a dense interconnect network between CMOS circuits. A wafer level approach, that has strong interest for future development of 3D integration and a chip level approach that is more attractive in terms of potential industrial applications (heterogeneous integration). During ***High Tree***, many process steps have been tested such as molecular wafer-to-wafer bonding, wafer alignment, wafer thinning, wafer metal planarization and advance CMP techniques. For chip level 3D assembly, a novel packaging solution has been exploited. It consists of two chips glued together with a very thin acrylate-based adhesive in a 3D face-to-face configuration that leaves uncovered the standard I/O pads to have compatibility with the conventional wire bond technique.
For the second objective, two innovative technologies have been explored:

1. The use of surface tension of liquid solder bumps to create a self-alignment effect
2. The use of an active alignment technique based on capacitive sensors on-chip

The project has achieved important results with a number of "firsts", proof-of-concept demonstrations showing the potential of the technology:

- Design fabrication of the first microelectronic chip prototype with different cluster of capacitive electrodes in 0.13µm technology. The chip integrates array of capacitive electrodes with size of 25µm x 25µm, 15µm x15µm and 8µm x 8µm (one order of magnitude less area than capacitive interconnect state-of the art). A set of cells that enables high speed data and clock inter-chip communication with very low-power consumption using synchronous and asynchronous approach (around 1 Gb/sec for data for each channels and around 2 Gb/sec for clock with a power consumption of 0.14mW/Gps).
- Design fabrication in 0.13µm technology of an innovative multi-axis alignment measurement system based on integrated on-chip capacitive sensors enable to determine displacement along X-axis , Y-axis, Z-axis and both tilt and rotation with very high accuracy (less than 1µm).
- Innovative 3D chip packaging technique. Two chips have been assembled in a stacked 3D face-to-face configuration with high accuracy alignment and very thin adhesive layer gluing them. The stacked 3D chips have been wire bonding to a printed circuit board using chip on board approach (wire bond through a cavity).
- An innovative technology approach has been developed. It is able to support capacitive interconnections between two wafers fabricated in advanced CMOS process. Five key technologies have been involved and tuning for the

dense capacitive interconnects networks. Wafer-to-wafer molecular bonding, wafer-to-wafer alignment with accuracy less than 1µm, Wafer thinning less than 10 µm, etching, metallization and planarization, through silicon vias opening.

From our knowledge, It is the first time that worldwide this complete 3D process flow with processed

The results of the project have been submitted and accepted to top level international conferences (ESSCIRC, CICC, AMC, and ECS). Three patents are pending and the main results have been presented to product division of ST for exploitation in future industrial applications.

The consortium composition and roles have been as follows:
ARCES (I) – Coordination, Physical simulation and modelling, system level design, circuit design, silicon design, preliminary testing, testing board design, chip design prototyping, capacitive sensors physical and electrical characterization , sensors design , active alignment testing validation.
CEA-LETI (F) – Development of the 3D bonding wafer process (wafer to wafer molecular bonding, Wafer alignment with aligner and optical tool, CMP and metal planarization, topology surface characterization, wafers grinding, photo lithography for backside alignment marks, Oxide deposition, I/O vias etching). For self alignment process development: solder bumps fabrication, metal etching and cavities fabrication, test vehicle design and fabrication.
STMicroelectronics (I and F) – Silicon fabrication, CMOS 130nm standard digital library, I/O standard library, device models, circuits design PLL, process development support (passivation surface modifications, morphological silicon wafers for process tuning, equipments: Scan Electron Microscope, probe station, aligner machine), electrical packaging, alignment circuits design.

Project objectives

This project has studied and investigated an enabling technology for high-speed three-dimensional chip-to-chip communication. Two are the main goals of this proposal:

- To study and implement 3D interconnection technology compatible with advanced CMOS process.
- To study and implement a 3D methodology of alignment that supports the interconnection approach proposed.

Methodologies and description of work

The approach developed in ***High Tree*** project is based on wireless capacitive coupling technology. The idea consists of placing two ICs in a 3D stacked front-to-front configuration in such a way that a common surface between each pair of two opposite chip surfaces is created. The chip surface bears a two-dimensional array of micro-locations. Capacitors are created with electrodes made in the top metal layer and using as dielectric the oxide silicon passivation in the top of the IC. These electrodes are properly energised to create temporal variations of the electric field on the chip surface. This induces a suitable electric field in the spatial region above each micro-site in correspondence of the other micro-electrode; communication takes place by capacitive coupling. This kind of wireless interconnection communication scheme offers many advantages:

1. Non-contacting AC connections can be built in a simpler and denser than DC connections (bumps)
2. Capacitive AC coupling offers better performance (speed and power) than standard I/O pins
3. Capacitive AC interconnect are reliable and scalable with technology node
4. Capacitive interconnects require minimum area (no ESD protections)

The communication scheme proposed in ***High Tree*** project enables to achieve high data rates exploiting synchronous and asynchronous techniques. Different circuit topologies have been proposed and they significantly advance the state-of-the-art in term of performances (two patents are pending for this solution).

The proposed communication scheme is:

- Extremely compact in terms of area with 64μm^2 /pin. It is 1/150 smaller than standard I/O pins in 0.13µm technology, 1/ 3 less then state-of-the-art of capacitive interconnects [1].
- Very low-power approach. It has a power dissipation 1/300 versus standard I/O e two-orders of magnitude less than state-of-the-art [2, 3].
- Bandwidth density (maximum bit-rate/electrode area) more than 2 times with respect the state-of-the-art [3].

In ***High Tree*** project new 3D assembly and packaging technology concept have been demonstrated.
A dense network of capacitive interconnects between CMOS has been implemented combining molecular wafer-to-wafer bonding with monitored alignment. All technological steps used are compatible with advanced CMOS technology process. The basic process steps, which were developed for 3 D integration, include:

- Dielectric deposition and planarization
- Precise wafer-to-wafer alignment
- Molecular direct wafer bonding
- Wafer cleaning and thinning up to 10µm
- Back-side aligned photolithography
- Through thin silicon vias etching

These experiments address several key points for future development of 3D integration and its industrial application:

1. To get the best alignment it is mandatory to follow a design symmetry at wafer level and chip level (common size, common from factor devices ex. Memories)
2. The topology should be as low as possible in order to minimize the final oxide thickness in homogeneity induced by CMP planarization step (better planar damascene metallization Copper than Aluminum)
3. The topology at the last metal layer has to be designed in a way to allow IO vias opening only in dielectric stack.

From our knowledge, It is the first time that worldwide this complete 3D process flow is realized

In ***High Tree*** project a new 3D chip packaging solution has been proposed. Two un-passivated chips have been stacked in a 3D front-to-front configuration using acrylate adhesive layer as inter-electrode dielectric and to provide mechanical stability with 1µm of alignment accuracy and 750nm of inter-chip spacing. The stacked chips are placed in a proper printed circuit board and a Chip-on-board approach has been adapted a standard wire bond technique.

In ***High Tree*** project innovative aspects in the field of alignment have been carried out. Two approaches have been investigated:

1. The self alignment technique based on solder bumps. The surface tension between the melted bumps and the pads directly facing the bumps creates a self-alignment of the two structures. For the purpose of this project not only a good alignment must be obtained after assembly but also a close contact between the two surfaces of the capacitive interconnection areas. This approach has exploited innovative aspects of solder bumps technology and melted metals properties.

2. The active alignment based on the idea of introducing on-chip sensors that can detect the relative alignment of the two chips facing each other.

In the active alignment an innovative solution has been proposed during this project (1 patent is pending on this solution). It has been proposed a multi-axis measurement system that evaluates displacement in X-axis, Y-axis, and Z-axis and at the same time provide information for tilt and rotation with accuracy about of 1µm. New capacitive on-chip sensors have been designed to provide information about displacement. A test chip has been fabricated in 0.13µm, 6 metal standard CMOS process to test the multi-axis alignment system based on 3D sensors. A capacitive charge variation of 1fF over 15fF corresponding to a resolution accuracy of 0.5µm over a range of 50µm has been measured. Sensors area is 120µm x 30µm and their power consumption is 200µW.

World-wide "state-of-the-art" updates

Many research activities and start-up companies are focusing their activities in the 3D integration field. They proposed many different technology options to make possible 3D integration of devices.
There are also different proposal for 3D interconnect at the moment, the comparison of various form of interconnect and the prediction on who wins the technology race are still too early to tell. There is an increased awareness in the industry that 3D integration will be a differentiator in future heterogeneous system product.

- ***Tezzaron*** (www.tezzaron.com) it is a US company that proposes a 3D stacking technology based on multi-wafer stacks approach. Tezzaron patented stacking process begins metallizing the wafers (the wafer is coated with SiO_2 and small pad of Cu are built). Two metallized wafers are optically aligned and then bonded together with a thermal bonding diffusion process producing a metal-to-metal bond. The backside of the upper wafer is then thinned (10µm). Vertical "Super-Vias" are built to connect the wafers. Tezzaron is actively seeking industrial and investments relationships.

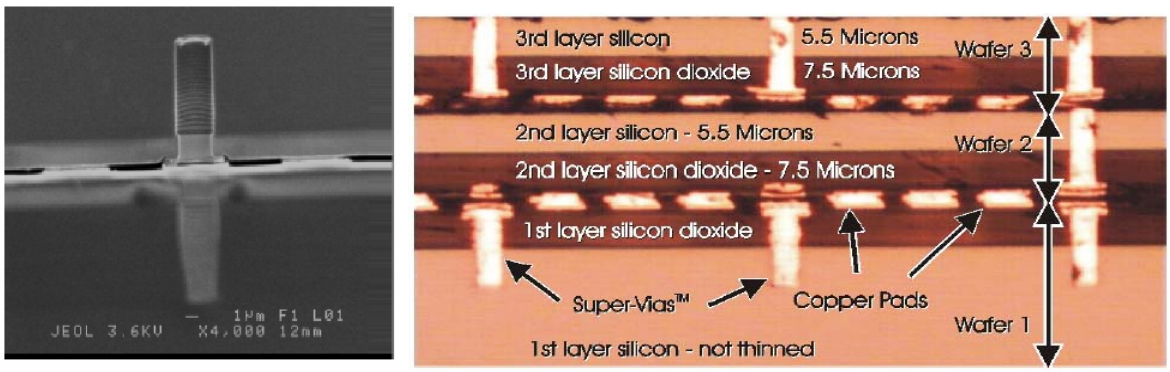


Figure 1: FAStack "Super-Via" Tezzaron technology

- ***Ziptronix*** (www.ziptronix.com) was spun out from North Carolina Research Triangle Institute USA. They have developed a technology for wafer-to-wafer bonding and die-to-wafer bonding with a patented process for

interconnections. A basic high-level process overview is reported here to provide a resultant 3-D structure placed in industry standard packaging for shipment to customer:

- CMP technique to planarize the materials
- Wafer and/or die surfaces are activated using standard chemical processes
- High High-speed pick and place are used to achieve aligned die-to-wafer bonding
- Covalent bonds between materials are created at room temperature without adhesives
- Thinning of layers - to within 10u if desired –
- Standard via and metallization techniques are applied to interconnect layers

- ***ZyCube*** (www.zy-cube.com) is a start up company with strong research collaboration between ASET Japan and Tokyo University. In ZyCube`s technology trenches used as the via-holes for vertically conducting electrical signal. These are created in chips or wafers that have to be stacked, and the conducting material is filled in these trenches. Then, chips or wafers are polished thinly and micro-bump electrodes are created on each surface to connect chips or wafers. On the surface of chip, other chips or wafer can be stacked and electrically and mechanically connected one with each other. Thickness of the stacked layer and the diameter of via-hole are adjusted to be in range from 10nms to 100nms, and in range from 0.5μm to 10μms, respectively. Tungsten or poly-silicon is utilized as the wiring material that fills the via-hole.

General 3D activities

- **Wafer-Level 3-D Activities**
  1. Rensselaer Polytechnic Institute RPI (monolithic 3D integration)
  2. MIT (wafer-scale 3D-ICs)
  3. Stanford (TFT in IC interconnects)
  4. Georgia Institute of technology GIT (3D theoretical simulation + architectures)
  5. Tohoku U. Tokyo (3D memory + imaging)
  6. IBM US (3D process interconnect)
  7. Arkansas Univerity (3D ICs for sensors)
  8. TraciT technologies France (SOI, 3D wafer bonding)
  9. Fraunhofer Inst/Infineon , Germany (3D ICs)
  10. IMEC/Intel (3D ICs and Ultra thin chip stacking)
- **3D Packaging**
  1. 3D Plus, France (3D memory/system in packaging)
  2. Tru-Si technologies Inc US (3D stacked wafer packaging)
  3. Irvine Sensors Corp US (3D-die stack)
  4. Amkor (3D system in package)
  5. Tessera (3D system in package)
  6. Xanoptix (3D Advanced analog RF , MEMs packaging solution)
  7. Sun Inc US (3D packaging and high speed interconnect)

High Tree project results offer validation to a new system-level interconnection technology with a strong impact on fields where power dissipation and performance are relevant, with a modest impact on the cost of the applications. A discussion is on going to start with the industrial partner (STMicroelectronics) the commercial exploitation of this technology. More ambitious application ideas are under discussion and could be submitted in near future.

1. Project results and achievements

Assessment of project results and achievements – Project's Achievements Fiche

Questions about project's outcomes	Number	Comments
1. Scientific and technological achievements of the project (and why are they so ?)		
Question 1.1. Which is the 'Breakthrough' or 'real' innovation achieved in the considered period	N/A	**What:** The test-chip demonstrates the possibility to transmit and receive data through AC connections at high bit -rate with very low power consumption and using very small capacitive electrodes. **Why:** This technique aims to miniaturize the overall volume of the application, increase bandwidth, reduce pin costs and alleviate heat problems. Such results promise a new generation of industrial

		products. **What:** First demonstration of a full process flow that enables to support capacitive interconnections between two wafers fabricated separately. **Why:** The development of this technology opens the possibility to integrate devices using a new 3D technology approach.
2. Impact on Science and Technology: Scientific Publications in scientific magazines		
Question 2.1. Scientific or technical publications on reviewed journals and conferences	4 papers	See references section for a complete list.
Question 2.2. Scientific or technical publications on non-reviewed journals and conferences		Dissemination is going to start inside STMicroelectronics product division. In July an ST workshop will include a presentation of High Tree project results
Question 2.3. Invited papers published in scientific or technical journal or conference.		The results will be presented in the next months to International Conferences.
3. Impact on Innovation and Micro-economy		
A – Patents		
Question 3.1. Patents filed and pending	3 patents pending	When and in which country(ies): filed in April still pending Brief explanation of the field covered by the patent: 1. Active alignment: analog closed loop system for measure capacitive electrodes displacement 2. Synchronous transmitter and receiver circuit for chip-to-chip communication 3. Asynchronous approach for data and clock transmission
Question 3.2. Patents awarded	0	Patent analysis under study : Many ideas for 3D packaging
Question 3.3. Patents sold	0	When and in which country(ies): Brief explanation of the field covered by the patent* (if different from above):
Questions about project's outcomes	**Number**	**Comments or suggestions for further investigation**
B - Start-ups		
Question 3.4. Creation of start-up	No	
Question 3.5. Creation of new department of research (ie: organisational change)	No	Name of department and institution/company:
C – Technology transfer of project's results		
Question 3.6.		

Collaboration/ partnership with a company ?		Which partner : STMicroelectronics Which company : STMicroelectronics What kind of collaboration? partner in this project and wide collaboration in many research fields
4. Other effects		
A - Participation to Conferences/Symposium/Workshops or other dissemination events		
Question 4.1. Active participation[1] to Conferences in EU Member states, Candidate countries / NAS. (specify if one partner or "collaborative" between partners)		Names/ Dates/ Subject area / Country:
Question 4.2. Active participation to Conferences outside the above countries (specify if one partner or "collaborative" between partners)		Names/ Dates/ Subject area / Country:
B – Training effect		
Question 4.3. Number of PhD students hired for project's completion	3	In what field: Electrical Engineering
Questions about project's outcomes	**Number**	**Comments or suggestions for further investigation**
C - Public Visibility		
Question 4.4. Media appearances and general publications (articles, press releases, etc.)	0	
Question 4.5. Web-pages created or other web-site links related to the project	1	www.hightree.arces.unibo.it
Question 4.6. Video produced or other dissemination material	No	
Question 4.7. Key pictures of results		References: (Please attach relevant material .jpeg or .gif)
D - Spill-over effects		

[1] 'Active Participation' in the means of organising a workshop / session / stand / exhibition directly related to the project (apart from events presented in section 2).

Question 4.8. Any spill-over to national programs	Yes	If YES, which national programme(s): Fondo Italiano per la Ricerca di Base (FIRB) - Project Funded by Italian Ministry of Research & University (MIUR) Progetti di Rilevante Interesse Nazionale PRIN - Project Funded by Italian Ministry of Res. & Univ.
Question 4.9. Any spill-over to another part of EU IST Programme.	No	
Question 4.10. Are other team(s) involved in the same type of research as the one in your project ?	No	If YES, which organisation(s): See References and list in the section " world update of state-of art"

2. Workpackage List and Deliverables summary sheet

Deliverable No	Deliverable Title	Delivery Date	Nature	Dissemination Level
D1.1	Report on physical models of cells for communication	T0+3	R	RE
D1.2	Report on electrical models of cells for communication	T0+6	R	RE
D1.3	Cell library Layout for communication	T0+9	O	CO
D1.4	Report on electric tests	T0+14	R	RE
D2.1	System level model of communication cell	T0+9	O	CO
D2.2	Report on chip architecture for full speed test	T0+15	R	RE
D2.3	Layout of chip level demonstrator	T0+20	O	CO
D2.4	Report of procedures test	T0+30	R	RE
D3.1	Wafer Bonding for capacitive interconnects	T0+12	P	CO
D3.2	Wafer bonded interconnect basic cell demonstrator	T0+15	P	CO
D3.3	Final report on Wafer bonding capacitive interconnects	T0+30	R	RE
D3.4	Demonstrator of interconnect System	T0+30	D	CO
D4.1	Cell layout for active alignment	T0+9	O	CO
D4.2	Report on self-alignment	T0+12	R	RE
D4.3	Report on testing of active alignment	T0+26	R	CO

D4.4	Final Report on self-alignment technology	T0+30	R	CO
D5.01	Project Presentation	T0+3	R	RE
D5.02	Dissemination and Use Plan	T0+6	R	RE
D5.03	Project Report	T0+12	R	RE
D5.04	Technology Implementation Plan	T0+30	R	RE
D5.1	Final Project Report	T0+30	R	RE

Yellow is technology objectives covered mainly by CEA-Leti

Green is system and circuit design objectives covered mainly by UNIBO and STM

Deliverable numbers in order of delivery dates: D1 – Dn
Month in which the deliverables will be available. Month 0 marking the start of the project, and all delivery dates being relative to this start date.
Please indicate the nature of the deliverable using one of the following codes:

R = Report
P = Prototype
D = Demonstrator
O = Other

Please indicate the dissemination level using one of the following codes:

PU = Public
PP = Restricted to other programme participants (including the Commission Services).
RE = Restricted to a group specified by the consortium (including the Commission Services).
CO = Confidential, only for members of the consortium (including the Commission Services).

3. Deliverable Summary Sheet

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-38931

Project Acronym: High Tree

Title: High-Speed Three-Dimensional Chip-to-Chip Communication

Deliverable N°: **D1.1; D1.2; D 1.3; D1.4** (WP1 see for details single deliverables reports)

Due date: T0+14

Delivery Date: T0+14

Short Description:

D1.1) The activity aims at estimating the values of the electric field between parallel plates and the related value of the capacitor, by varying the physical parameters here involved. This has led to demonstrate the feasibility of inter-chip capacitive communication through clusters of capacitive cells which are designed and manufactured exploiting the upper metal layer of a standard CMOS technology process. An exhaustive set of simulations has been carried out in order to estimate the dependence of the electric field generated between two parallel plates by varying their width and their mutual distance, as well as the dielectric constant, the metal plate thickness and the electrode-to-mass distance.

D1.2) The activity aims at evaluating the proper electrical models for the basic circuit blocks which are involved in the signal exchange between the two active layers, whether logic or timing signals. The main issues that have been explored are:

- high-speed circuits: in order to reach a very high bandwidth in the data exchange between the two layers, the parallelism in term of capacitive channels must be combined with high-speed design of internal building blocks
- Level-to-edge conversion: the capacitive transmission of the data necessarily requires a conversion from steady-state positive (negative) logic value into falling (rising) edge 50%-duty-cycle signal. This is achieved by multiplexing the data to be transmitted with its complement, using the clock as select signal of the multiplexer.
- Synchronous vs. asynchronous approach: the logic blocks working on the two layers must be synchronized to each other. This may be achieved:

  1. Sending a synchronization signal on a dedicated channel
  2. Regenerating the synchronization signal from the received data on the second chip.

D1.3) A library with the schematic and layout of cells for chip-to-chip communication has been designed and implemented in 130nm STMicroelectronics technology. Main cells are:

The layout of the True-Single-Phase-Clock (TSPC) D-FF is the basic brick of every synchronous system on the chip.

The layout of the receiver consists of an inverter biased at the logic threshold, thus acting as an amplifier of the received signal. The signal is then sampled by a standard TSPC D-FF.

The layout of the transmitter and the macro blocks (capacitive cell + receiver) are grouped into the same cluster with digital counters and registers

The 130nm layouts have been drawn by means of the first 2 metal layers only: this makes it feasible to accomplish a technological porting of the macro-block into Design Kits where a reduced number of metal layers are supported.

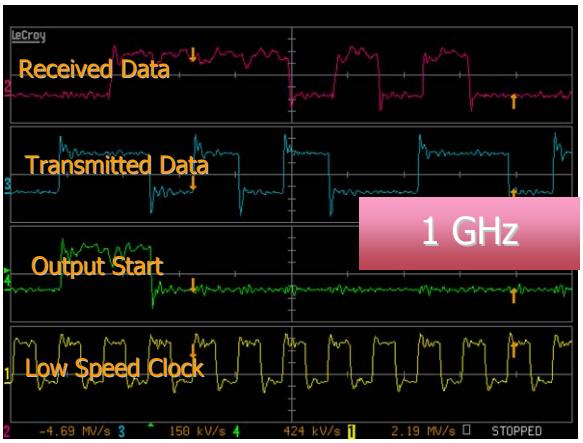
D1.4) A first test chip has been designed and fabricated in 130nm STMicroelectronics technology. It includes:

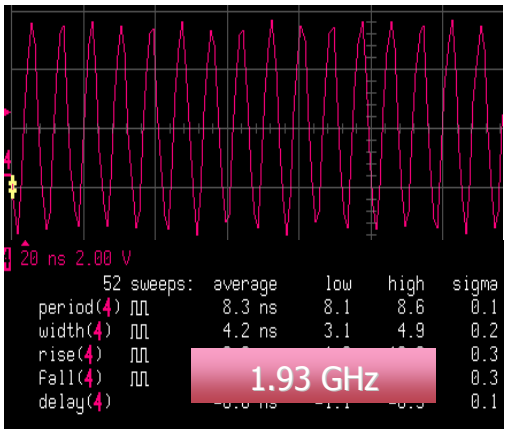
Clusters of different sizes of capacitive communication cells (25 μm x 25 μm, 15 μm x 15 μm, 8 μm x 8 μm)

On-chip clock generation (PLL). Another structure emulates in two-dimensions the capacitive communication channels exploiting interlayer capacitances and using the existing inter-metal layers to create capacitors. IO pad frame has been designed to make possible the wafer-t o-wafer assembly process. The test-chip includes also active circuits to test the alignment.

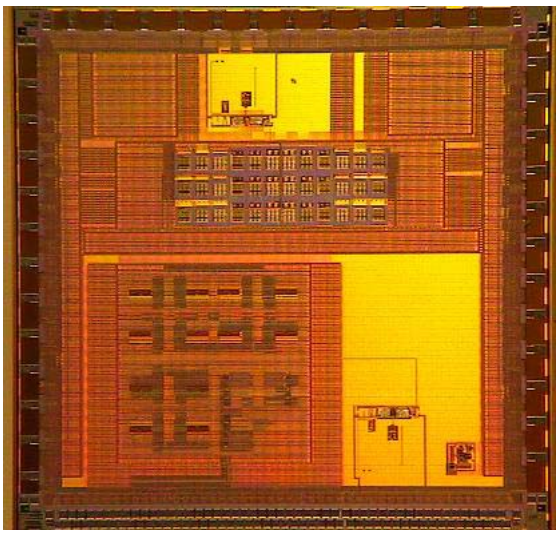
Main results:
Two dimensional structure have been tested (they have been tested at full speed)
The clock transmission cell has been measured and good functionality has been shown at working frequency of 1.2GHz
The data transmission shows that data are sampled and transmitted at 1GHz
Three dimensional structure has been tested electrical measurement confirms that the entire structure works properly. It has been tested at low frequency (25MHz)

Test frequency: 10-25 MHz for functionality. All clusters have been measured.





Test chip in 130nm, 6 metal level STMicroelectronics technology bonded in a standard PGA 256 pins ceramic package to test the two-dimensional structure. Wafers with the same test-chip have been used for process development of 3D technology. The test chip is 4.5mm^2 x 4.5mm^2 with symmetric core and asymmetric pad frame for wafer-to-wafer bonding.



Partners owning: ARCES-University of Bologna

Partners contributed: STMicroelectronics

Made available to: STMicroelectronics, CEA-Leti

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-38931

Project Acronym: High Tree

Title: High-Speed Three-Dimensional Chip-to-Chip Communication

Deliverable N°: **D2-1; D2.2; D2.3; D2.4 (WP2 see for details single deliverables reports)**

Due date: T0+30

Delivery Date: T0+30

Short Description:

D2.1) The development of a system level model describing the cell at HDL level, providing a synthesized version of the cell compatible with a standard cell library of the proper technology and with timing constraints, has been carried out. The system level model of the receiver simply consists of a standard flip-flop sampling on the rising edge of the receive-clock. The effects of the capacitive cell and of the analog blocks have been modelled as a delay line. The .lib and .db files have been generated for the timing characterization: the capacitance and time values refer to the characterization files of standard cells in HCMOS 0.13 um Technology Process. They can be easily modified to make the description more adherent to the actual performance of the full-custom macro cell or in case of technology migration.

D2.2) The objectives were the study, design and test of circuits that demonstrates the speed performance of the capacitive coupling communication approach. A test structure has been implemented for full speed testing. Since the maximum simulated working frequency of the communication structure is about 1.1GHz, an on chip synchronization protocol is required. As consequence, the basic full speed communication cluster includes:

1) A dedicated clock transmission channel (the synchronization signal is propagated from the receiver chip to the transmitter one)

2) An initialization channel (a standard communication cell used for the synchronization of the test structures)

3) 9 data channels for test pattern propagation (arranged in 3 x 3 matrix for cross talk verification)

Different communication clusters have been implemented with electrodes of different sizes for a complete characterization of communication performances. Moreover, high-performance input/output interface has been implemented, in order to force suitable test patterns through the capacitive cells, and also to verify received data. The input interface has a 9bit parallelism to fit the 3x3 organization of the basic communication structure; the test pattern are forced from IO pads and stored in a first level shift register structure: 8 vectors of 9bit are in sequence inserted in 8 registers connected to form a shift register with 9bit of parallelism and a 8 stages depth. When the input operation is over the test vectors are loaded in another high speed shift register structure; after loading, the 8 patterns are sequentially shifted at high speed through the capacitive cells for full-speed transmission. The output interface receives high speed vectors from communication channels (shifts-in 8 vectors from communication cells, starting with the initialization signal). The received 9bit vectors can be loaded on an output low speed shift register, for transmission verification. The structures have been implemented for three dimensional testing with electrodes sizes from 8x8 to 25x25 um2. A single-chip emulation has been verified a 1.1Gbit/sec/pin maximum bandwidth.

D2.3) The activity has been carried out in collaboration with STMicroelectronics. The design platform for the 0.13um CMOS process has been used to design a library of cells that enables to test the full speed of the communication channel. The main issues dealt with were:

1) Redesign of a custom I/O that enables to assembly the two chips in a stacking face-to-face configuration.

2) Design of schematic and layout of structures to evaluate the communication performances at full speed.

3) Floor plan and place and route of a full chip that enables to measure the performances in term of speed and power dissipation of different clusters of capacitive cells. Main cells designed:

Layouts and schematic for I/O pads (Input pads, output pads, Three-state pads, Bidirectional pads)

layouts of digital cells such as flip-flop, multiplexer, standard logic gate (inverters , buffers, nand, nor)

Some of these cells have been used in the full speed interface and must be carefully designed to support GHz frequency operation condition in order to avoid discharge in critical nodes and also to prevent unexpected coupling and cross-talk noise with adjacent lines. The load of the critical lines have been taken in account for sizing the buffers in order to reach the required speed performances. A proper clock tree has been designed for synchronization of the whole the system. Since the design methodology has required the design of integrated circuits of a sizable complexity, a system level description and a digital design flow has been introduced in order to produce results within the specified time constraints. Parasitic extraction from layout and simulations has been implemented to show the robustness of the design.

D 2.4) The activities that have been carried out consist in the design and implementation of an entire system that enables to support inter-chip full speed communication using a dense capacitive interconnect network (cells library layouts were developed in the previous deliverable).

A test chip in 130nm STMicroelectronics technology has been fabricated. This test-chip includes:

1) The same communication structures of the previous test chip designed for wafer-to-wafer assembly (deliverables D.1.3 workpackage1). It contains clusters of capacitive cells of different size: 25µm x 25µm, 15µm x 15µm, 8µm x 8µm. The electrodes are made in the topmost metal layer (in ST process copper is last metal layer but to be able to wire bond with traditional tools and technology , aluminum is place on the top of each standard I/O pads). Due to this constraint also the capacitive electrodes of copper are covered by aluminum and connected by vias. Moreover, aluminum in ST advanced CMOS process is not assembled with a planar damascene process as copper metal6 but is not planar. To compensate the surface topology, several experiments have been carried out in collaboration between ST and CEA-Leti to make compatible the surface flatness and roughness for assembly technology. Transmitter circuits and receivers have been designed for a full speed synchronous approach for data and asynchronous for clock. The design has been carried out using standard digital design methodology (we use same pitch of the logic cells of ST library to integrate the new capacitive interconnect using standard cad tools for Place and route in a Back-end digital flow).

2) As BIST and BER structures we have reused the schemes designed in the first test-chip and already tested.

3) PLL for on-chip clock generation has been integrated to test speed performance

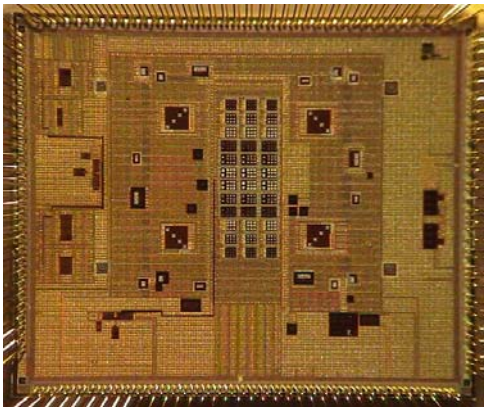
4) The chip includes the last version of active alignment circuits and multi-axis measurement system of alignment developed in WP4

5) I/O pad frame supports the chip-to-chip assembly. It has been designed in one single side.

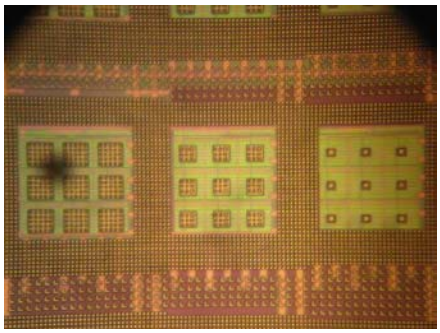
The floor plan of the chip has the same symmetry axis in the core structure to allow the front-to-front stacking of the receiver on one side and the transmitter on the opposite one. To test this prototype we have outsourced its fabrication to IZM-Fraunhofer. It has developed a packaging solution that stacks two chips together in 3D face-to-face configuration with 1µm of alignment accuracy. The chip symmetry axis is designed in order to leave the two chips displaced (600µm) with the IO sides uncovered (this is because it is necessary to access for testing reasons the standard pinout). An acrylate-based adhesive provides the inter-electrode dielectric and mechanical stability (The SiO_2 passivation was not deposited on the die the process was stopped after aluminum deposition). The thickness of the glue between chips is around 750nm. A prototype demo board has been designed to test the 3D chips stack. It is a standard Printed circuit board (PCB) with 4 layers where the chip-stack is mounted with innovative approach by means of Chip-on-board technology. The bottom chip is wire bonded with conventional technique while the upper-one is bonded through a cavity to the opposite site of the underlying structure (see figures section for details).

For testing purposes, a wire-wrap board has been implemented. This mentioned board realizes a flexible interface between the chip-stack and the measurement setup (pattern generator, oscilloscope, power supply, acquisition board).To test the system, patterns are generated by pattern-generator equipment, or from an acquisition board with FPGA devices. The results of transmission have been displayed with an oscilloscope, or can be checked on the acquisition board. With this procedure the full functionality of 8x8 μm^2 (900Mbps/pin), 15x15 μm^2 (975Mbps/pin) and 25x25 μm^2 (795Mbps/pin) capacitive interconnection has been demonstrated. The 25x25 μm^2 channels have a reduced maximum-rate due to the parasitic involved in a larger electrode, the 8x8 μm^2 one have a rate reduction due to the reduced inter-electrode coupling. Power dissipation is in the first case 15uW static power and 0.13uW/MHz dynamic power, while in the second one is 23uW static and 0.1uW/MHz dynamic.

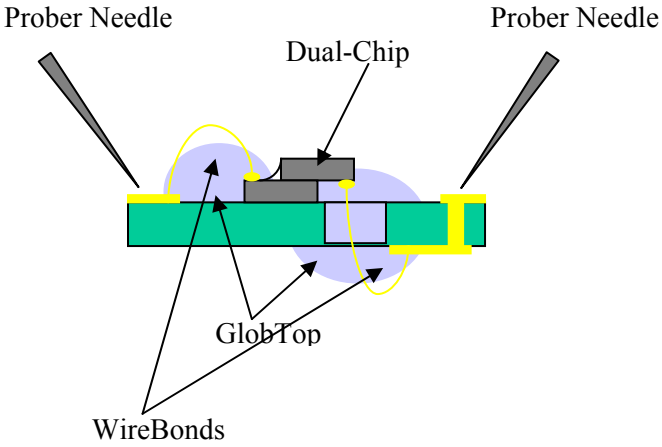
Test Chip for Full speed Inter-chip communication STMicroelectronics 130nm technology 6 metal 5mm x 5mm



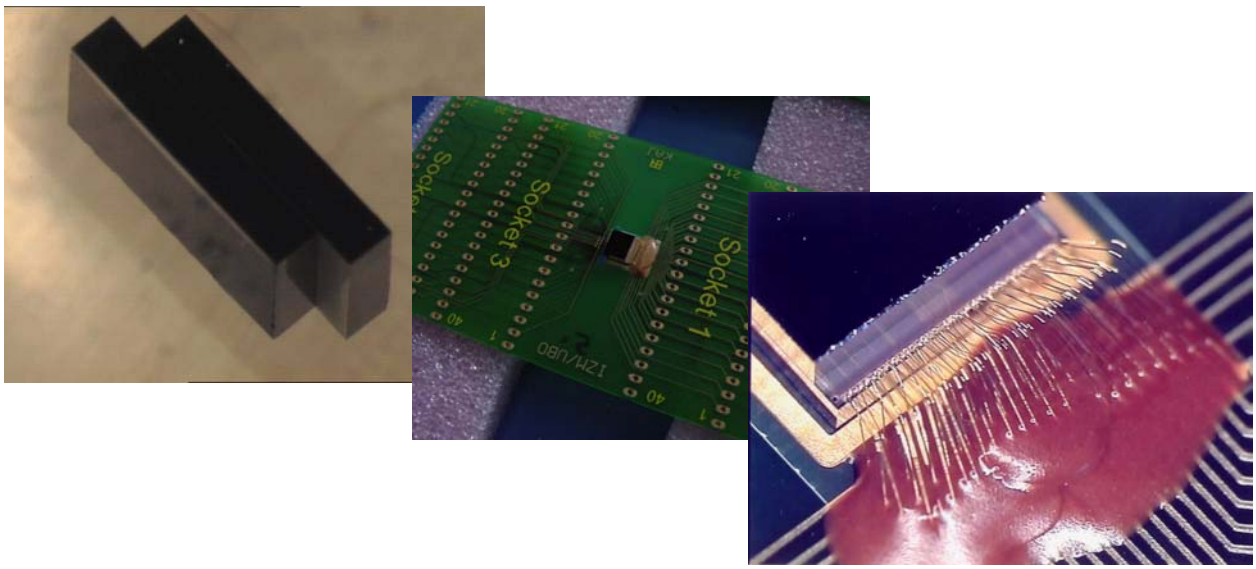
Clusters of capacitive cells with different sizes



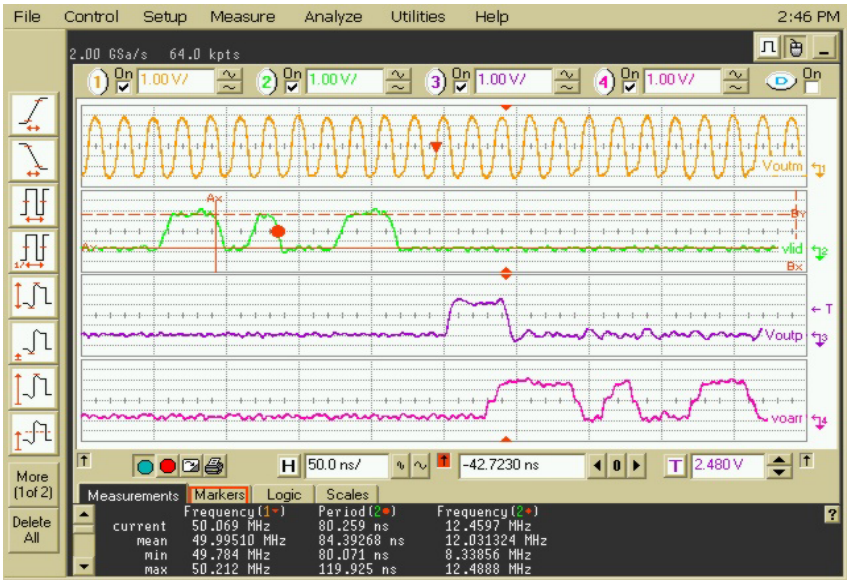
Demo board idea for testing of chip-stack



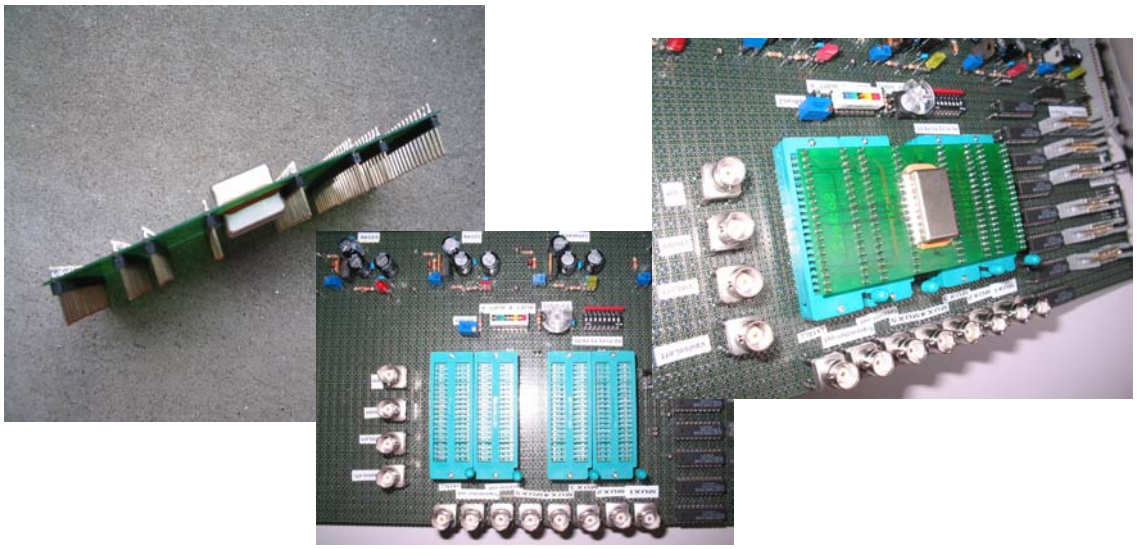
Two chip packaged in 3D stacking front-to-front configuration and PCB demo with Chip on board



Testing waveforms that demonstrate the full speed inter-chip 3D data and clock communication



Experimental testing setup board



Partners owning: ARCES-University of Bologna

Partners contributed: STMicroelectronics

Made available to: CEA-Leti

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-38931

Project Acronym: High Tree

Title: High-Speed Three-Dimensional Chip-to-Chip Communication

Deliverable N°: **D3.1; D3.2, D3.3; D3.4 (WP3 see for details single deliverables reports)**

Due date: T0+30

Delivery Date: T0+30

Short Description:

D3.1) wafer bonding to create capacitive interconnects (first intermediate status)

The main objective was to connect two CMOS processed wafers to create a dense 3D capacitive interconnections network. These capacitive interconnects are realized by two aluminum pads aligned and bonded front to front. A SiO_2 layer is used as bonding layer and it forms the dielectric. Morphological wafers were used for the first experiments of wafer bonding of CMOS processed wafers. The first process step that has been tuned is the planarization of the CMOS wafers. After surface characterization, the top SiO_2 layer of each wafer is planarized with CMP technique. SiO_2 removal rate and the homogeneity have been measured on dummy wafers. Then the remaining oxide thickness is measured directly on the pad using IR spectrometry. After cleaning the wafers are bonded together with an optical alignment. A thermal annealing around 200 ^{0}C is performed to strengthen the bonding. The first observations have shown that the topology and high oxide removal needed are not compatible with a good homogeneity of the final oxide thickness. As we try to reduce the oxide thickness down to 200nm, all the oxide was removed in the center of the wafer. As consequence only the edges of the wafers were bonded. This confirms that it will be needed to put more oxide in the top to reach a good planarization. A second set of experiments have been performed to solve the issues above mentioned. More (2µm) oxide layers were deposited on the top of the morphological wafers the total thickness has been controlled by spectrometry. It was shown that after CMP etch removal the removal rate was greater than the former one. Since it is difficult to have a precise measure of the oxide thickness it was decided for this experiment to let 400nm of SiO_2 on top of each wafer. To enhance the alignment of the two wafers a dedicated tool was used and a notch-to-notch approach has been implemented. An infrared microscope checks the alignment before to strengthen the bonding. In case of misalignment the wafers are debonded and the alignment is done again. *At the end a full wafer bonding was obtained and reproduced several times.*

D3.2) The experiments performed on morphological wafers have been extended to demonstrate the technology to connect two separately processed CMOS wafers. A set of wafers in 130nm STMicroelectronics technology were delivered. For a good progress in process flow application it has been necessary to evaluate the topology of the wafers (at last metal level and at passivation level for the STM HCMOS9 process).

Topological measurements of Aluminum structures were used based on profilometer surface scanning and SEM photo and FIB elaboration. Then a wafers preparation was performed for the needed symmetry required by face-to-face bonding. Wafers were first prepared by laser cutting to make two four inches wafers from an 8-in wafer. A solution to compensate the edges gap after chip alignment has been developed. A complete process flow for 3D integration has been elaborated. Main steps are:

1) Wafers cleaning (both sides)
2) Wafers marking (back side)
3) Nitride and partial PECVD oxide etching (front side)
4) PECVD oxide deposition (front side)
5) Photo litho alignment marks (back side)
6) Alignment verification (back/front sides)
7) Marks etching (back side)
8) SiO_2 CMP and thickness adjustment (front side)
9) Wafer bonding with annealing (both sides)

10) Silicon grinding (back side)

11) Photo litho via (back side)

12) Deep silicon etching (back side)

13) vias opening (back side)

14) Final verification (both side)

Many steps of this process flow needed a supplementary approach in process development before their application to the STMicroelectronics CMOS processed wafers. This was achieved using training silicon wafers for technology debugging and evaluation.

D3.3) and D3.4) To reach the target of a demonstrator for the capacitive technology interconnect, two mask levels for 3D structure realization are needed, the first one for the aligned face-to-face bonding step and the second one for the via I/O opening. This second mask level is applied on the thinned backside of one wafer by a pair bonded structure.

The new mask level must be aligned and coordinated with the frame and architecture of STM CMOS process mask with respect to the symmetry. Two concepts were imagined for via opening:

1) Common via opening for a line of pad extension .The schemes is available for more pads with extension.

2) One via opening for two pads

Highlights and main results:

During WP3, 3D integration was achieved for capacitive coupling structure implementation between two HCMOS wafers. The standard processed wafers were precisely aligned with ~1 µm accuracy for the best results and directly bonded via dielectric layer for the capacitance implementation. After a backside of the bonded sandwich wafer was thinned, the Input and Output via photolithography were backside aligned with good accuracy < 0.5µm and opened through the thinned Silicon and stacked HCMOS structure of both wafers. The access to the communication structure was prepared for the final packaging of integrated chips. The following technology has been developed:

a) Symmetry recovery by laser cutting of the wafers.

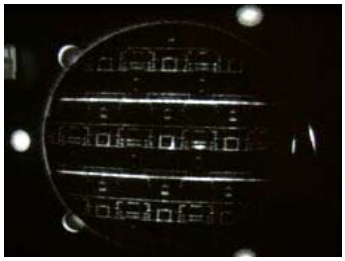
b) Planarization of huge topology 3 µm on HCMOS 9 wafers

c) Bonding of HCMOS processed wafers with alignment specifications

d) Via opening through 30 µm Si and 10 µm dielectric stack with a controlled etch stop on aluminum pads.

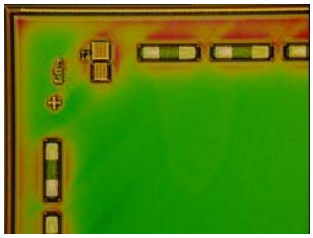
<u>From our knowledge, It is the first time worldwide that this complete 3Dtechnology is realized</u>

a)

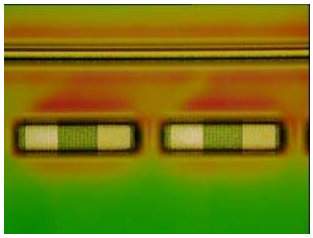


b)

HCMOS wafers after alignment and direct wafer bonding: a) optical view , b) infrared view

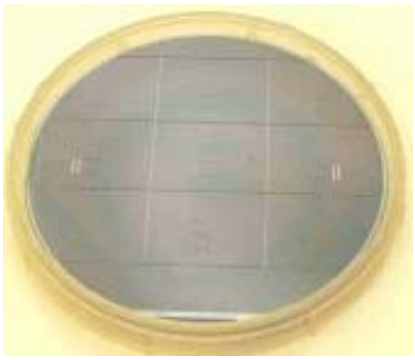


a)

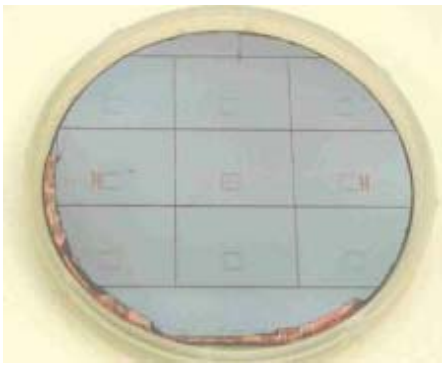


b)

Optical observation of the via opening at two levels of the Aluminum pad extension



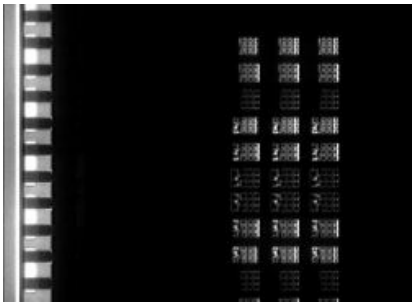
A)



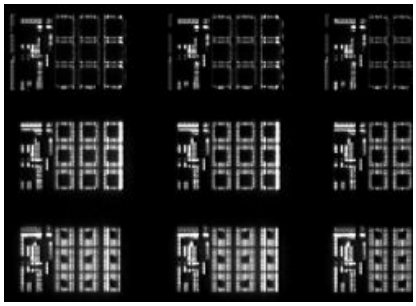
B)

A) Bonded HCMOS wafers after the photolithography mask step for input and output metal pads etching

B) Bonded HCMOS wafers after the complete vias opening through bare Silicon, the stacked HCMOS layers and bonding layers.



a)



b)

Infrared photos of the pads and opened vias area – left on photo -a) and aligned capacitances (right on the photo –a) and zoom photo -b)).

At this step the dies are available for electrical tests. We are performing the packaging for demonstrator

Partners owning: CEA-LETI

Partners contributed: STMicroelectronics

Made available to: ARCES-University of Bologna

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-38931

Project Acronym: High Tree

Title: High-Speed Three-Dimensional Chip-to-Chip Communication

Deliverable N°: **D4.1; D4.2; D4.3; D4.4 (see for details deliverables reports)**

Due date: T0+30

Delivery Date: T0+30

Short Description:

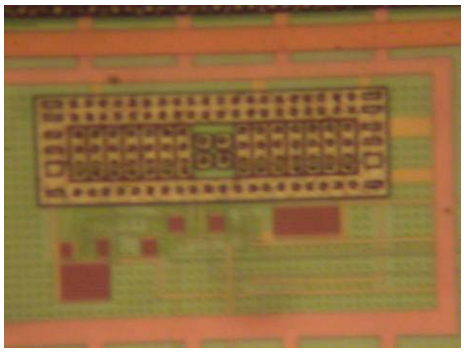
D4.1) ARCES/STMicroelectronics

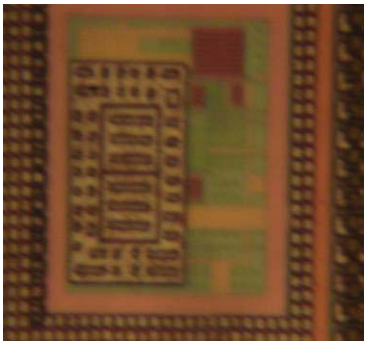
Following the idea of placing two o more structures in a 3D stacked front-to-front configuration, one of the main issues to maximize the signal to noise ratio is to achieve alignment of the capacitive electrodes with very precise accuracy. Careful alignment is extremely important when the area of the capacitors is extremely small. For this reason, an innovative technology has been explored to use capacitive measurement in order to provide information concerning the placement. CMOS circuits have been designed to test the active alignment technique. These circuits sense the capacitance created between two IC stacked in 3D configuration and provide a feed back to an external placement machine. A test chip with some of these circuits has been implemented in 0.13um ST CMOS technology and testing results have shown that the output value allows to measure a capacitance variation in the order of 1fF and a relative displacement in the range of 1 micrometer.

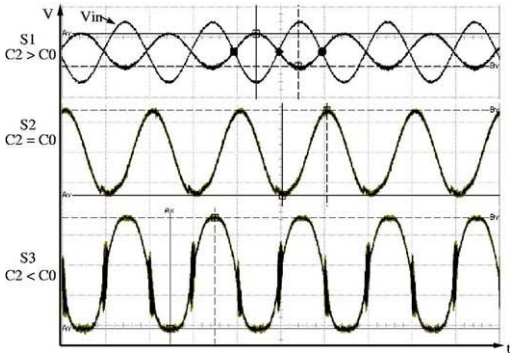
D4.3) ARCES/STMicroelectronics

To measure alignment along X or Y–axis, we have designed a capacitive sensor with a four-electrode scheme. The structure is formed overlying one electrode, located on a top die, over three electrodes placed on a bottom die. The bottom electrodes are made with the top metal layer while the upper-one is electrically insulated. The two dies are stacked together in a face-to-face configuration and the passivation layer of silicon oxide is used as dielectric. The multiple capacitors structure (C0, C1, and C2), formed between the top and bottom electrodes encodes the position information. The value of each capacitance, assuming a parallel plate model is then calculated from the equation $C = \varepsilon WL/d$ where W/d is the electrode width-to-separation ratio and L is the length. A shift of the upper electrode, along X or Y axis direction, changes the overlapping area and the capacitance values of C0 and C2. By means of an analog integrated read-out circuit not only the direction but also the entity of the displacement is determined. The same structure but with only three electrodes has been used to determine the spacing between the two chips. Two metal plates are placed on the bottom chip, and a third plate, placed in the top chip, is opposed and fully overlaps the bottom ones. The two bottom electrodes are connected separately to the input and output of a charge integrator. Since the feedback capacitance *C*z is inversely proportional to the vertical distance z while the output voltage of the charge amplifier is inversely proportional to the feedback capacitance value, a linear dependence of output voltage on vertical distance is expected. In perfect alignment configuration, the capacitance value C0 and C2 are the same, the op-amp works like a buffer, and as a result the two waveforms have the same amplitude. When the upper electrode is shifted over the input electrodes the sinusoidal output waveform has a bigger amplitude than the input one when C0 value is greater than C2, while on the opposite movement causes a sinusoidal output waveform with a lower amplitude than the input one (C0 value is less than C2). In the experimental setup, two chips have been aligned and misaligned of predefined values, using a micromanipulator, and then stacked and glued together in a face-to-face 3D configuration. Only the input/output pads of bottom chip have been wire bonded to provide the power supply and stimuli. The four-electrode sensor has been distributed along the perimeter on the chip plane to detect position information on X and Y direction. The three-electrode sensors are located in the four corners of the chip to enable measure of displacement in Z direction and also to provide tilt.

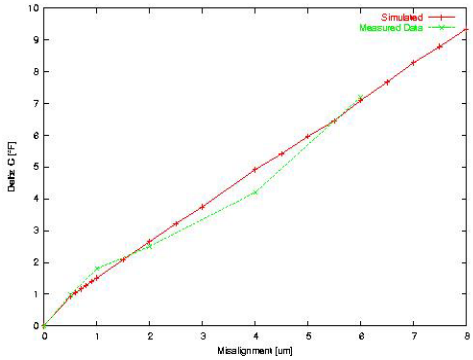
STMicroelectronics 130nm process: Capacitive sensors for alignment 4-electrodes structure and 3 electrodes scheme for tilt, rotation and Z-axis



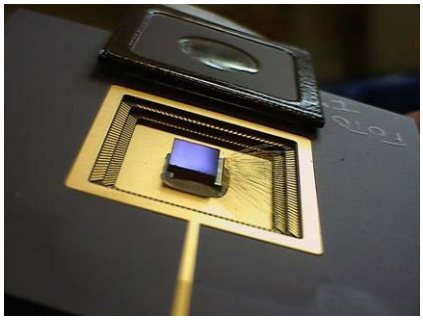




Measured output sensing voltage



Charge variation versus misalignment



To test the overall idea 3D stacked in a face-to-face configuration has been aligned and misaligned of predefined values and put a standard PGA 256 pins for electrical characterization

Highlights and main results

A multi-axis measurement alignment system for chip placed in a 3D face-to-face configuration has been proposed. A test chip in 0.13µm standard CMOS technology has been fabricated with on-chip capacitive sensors and alignment circuits. Each sensor has an area of 120µm x 30µm, the power consumption is 200µW.

Capacitive variation of 1fF over 15fF is evaluated corresponding to a resolution of 0.5µm over a range of 50µm.

D42.2) ; D4.4) CEA-Leti

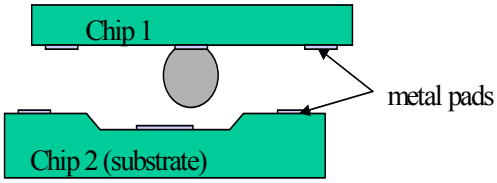
The solution investigated here is a self alignment technique based on solder bumps. The surface tension between the melted bumps and the pads directly facing the bumps creates a self-alignment of the two structures. It is known that alignment better than 1µm can be obtained with this type of assembly. The difficulty here is that not only a good alignment must be obtained after assembly but also a close contact between the two surfaces of the capacitive interconnection areas**.** Two main problems must be solved from a technological point of view:

1) Self-alignment and contact must be obtained at the same time

2) fluxless soldering must be developed to keep clean surfaces for oxide bonding

In Flip chip bonding, solder bumps are higher than several tens of micrometers. Thus, to obtain a contact between the two surfaces with the capacitive pads, the solder bumps must be made in cavities. To reduce the number of technological steps, the cavities can be made in only one chip. In this case, the solder bumps are only used for their mechanical properties (to obtain self-alignment) and not for an electrical contact. Thus, to consume a small die area, the diameter of the bumps must be as low as possible. For this size of bumps, electro deposition of solder must be used. As it is difficult to control with a high accuracy the height of the cavities and of the bumps on a whole wafer, standard flip-chip bonding is not suitable to obtain self-alignment and contact at the same time. Before assembly, flux is spread over the surface of the chip. During reflow, the flux vaporizes and deoxidizes the surface of the solder. After assembly, there are flux residues that must be cleaned to avoid reliability problems. In our case, fluxless soldering must be developed to have no residue on the oxide surfaces that will be in contact.

A specific test vehicle and associated masks were designed for the self-alignment study, to realize two types of chips on 100mm-diameter silicon wafers: one with solder bumps (called chip 1) and the other with cavities (called chip2 or substrate).



Eighteen structures were designed with different geometrical parameters (diameter and pitch of the bumps, number of bumps per chip, dimensions of the cavities). The diameter of the metallization on the bump side is 20µm (100µm pitch) or 50µm (200µm pitch). For each structure the chip is 6 mm large and 8 mm long, and the substrate is 8 mm large and 16 mm long.

For the substrate wafers two lots were processed with different cavity depths. Etching of the cavities is performed by a wet process (KOH etching). Thus, the cavities are pyramidal. After etching of the cavities, the UBM (Under Bump Metallurgy) is deposited on the substrate and etched. According to the wafers, the cavities are 11 or 14µm deep.

For the chip wafers two lots were processed with different bump heights. The solder alloy for the bumps is eutectic SnPb obtained by electrodeposition. Several bump heights were obtained between 12 µm and 40 µm according to the wafer.

After sawing of the chip and substrate wafers they are ready to be assembled. A first set of assembly was performed with fluxless soldering.

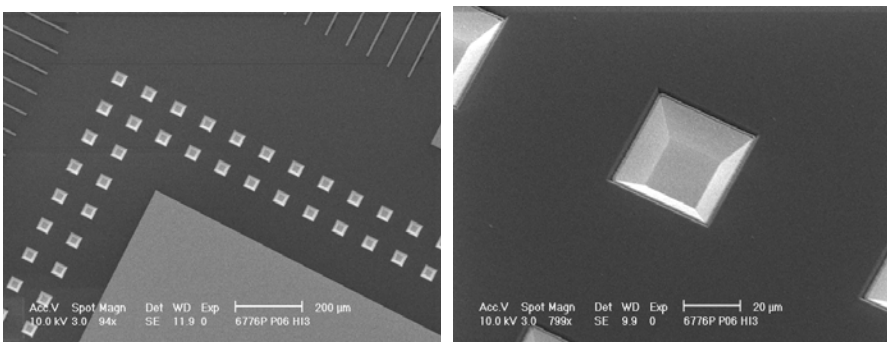
The conclusion of this first set of experiments is that with the fluxless soldering process used, the wetting of the solder is not always good and no self-alignment is obtained even with the reference structures. We obtained an alignment between 1µm and 7µm according to the samples. As no self-alignment was obtained with fluxless soldering, a second set of assemblies was performed with flux. As it is a more standard assembly technology, alignment results should be better because self-alignment should occur. This first step allows to validate the geometries and the concept of self-alignment with contact. In this second set of experiments, the air gap between the metal plates was reduced from 5µm to about 1µm.

Conclusions:

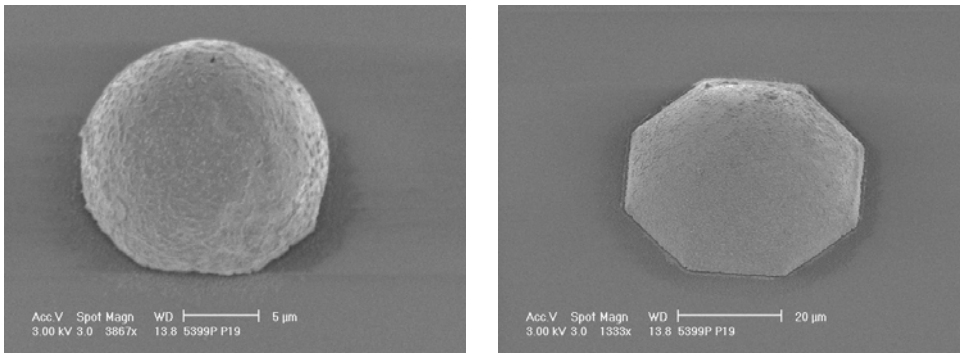
Since this technology was considered risky, we did not plan to rely on it to realize the demonstrators. In fact, it is very difficult to obtain self-alignment and contact at the same time.

Several concepts were selected and tested without success. However, as a good alignment is obtained when the under bump metallurgy has the same diameter for the substrate and chip pads, we can assume that an air gap of several micrometers can be achieved between two chips by controlling the cavity depth and the bump height.

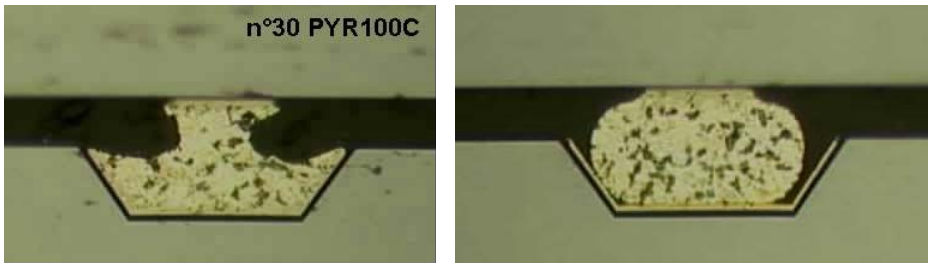
Metallized pyramidal cavities



Pad diameter 20 µm, bump height 22 µm **Pad diameter 50 µm, bump height 12 µm**



Solder bump in cavities after reflow. Cavity depth 11µm.



Partners owning: ARCES-University of Bologna/ STMicroelectronics/ CEA-Leti

Partners contributed: ARCES-University of Bologna / STMicroelectronics/ CEA-Leti

Made available to: All the partners

Potential Impact of project results

The ***High Tree*** project has demonstrated that an inter-chip data transmission based on AC capacitive coupling approach addresses several of the limitations of the traditional ohmic interconnect approach. An enabling technology has been developed to implement a dense network of interconnects between two wafers fabricated separately with advanced CMOS process. This network allows to design chip-to-chip communication that simplifies circuit design and reduces area and power requirements. This technology reduces pin pitch by an order of magnitude, improves the inter-chip bandwidth supporting multi-gigabit-per-second data rates and due to lower inter-chip capacitance significantly reduces the switching energy alleviating heat problems. Moreover thanks to low power and reduced pin area it makes this approach able to support a huge number of parallel communication channels without reliability degradation and to scale with the feature reduction of the VLSI technology. The different technologies developed in the frame of ***High Tree*** project have a great potential and prepare the 3D chip integration concept to industrial exploitation and future 3D product development. wafer-to-wafer molecular bonding , wafer-to-wafer alignment, planarization and etching, wafer thinning and through silicon vias etching are still the key technologies that offer the best way for future 3D system integration.

High accuracy alignment technologies have been also pursued in the ***High Tree.*** They offer advances in the current state-of the-art and promise potential impact both in the research field and industry. Accurate and very precise alignment is an issue of growing interest in system-in package application and for 3D integration. With conventional optical tools and alignment techniques in general, it is difficult to achieve the needed accuracy. Hence integrated capacitive sensors promise to meet the demand for low-cost, high resolution, high reproducibility measurement methods. Moreover, the use of surface tension liquid solder bumps to create self-alignment effect has strong interest for future development of 3D integration because it makes possible hundreds or thousands of precision alignments with a single batch reflow process. This improves the fields of application of this technology because the cost/alignment can be reduced by orders of magnitude. This could be particularly useful for 3D MEMs structures.

Future Outlook

The ***High Tree*** project proposes an enabling technology for high speed chip-to-chip communication. In this project we have investigated innovative 3D assembly process at wafer level and chip level. The technology that has been developed offers features that can be very useful to support system level innovation:

- High data rate, bandwidth, high parallelism, reduced power dissipation are essential to overcome the bottleneck of conventional interconnection in System-on-chip integration. Today, the processors ICs incorporate the processing unit and the first level cache. The second level cache consists of an array of static random access memory (SRAM) located next to processor. The main memory is composed of dynamic random access memory (DRAM) components. This implementation significantly impacts the performance of the memory hierarchy. Only a limited amount of area is available on the processor chip for caching so second-level caches are forced to be implemented externally. Access time is strongly impacted by signal transmission delay (off-chip slower than on-chip), and bus width is limited by pin constrains. Using High Tree 3D-technology a processor system may be implemented moving the second-level cache and main memory on one 3D-IC. This approach opens a wide range of potential applications in the fields of computing architectures.
- Wafer-to-wafer bonding and a dense capacitive interconnect networks offer many benefits for the memory product market. In several cellular phone applications, there is an increasing demand of combined Flash and SRAM modules to reduce footprint and power dissipation.
- In many RF applications one of the limiting factor in performance of RF circuits is due to parasitic losses caused by wire bonds since series inductance and shunt capacitance of wires reduce bandwidth and have to take in account for good impedance match. High Tree technology seems promising to overcome some of this issues since support it support heterogeneous technology integration and provides lower parasitic, better EMI, less heat dissipation low power circuits and thinned substrate to reduce thermal resistance.
- Reconfigurable computing is currently under investigation, in this kind of application high parallelism and high bandwidth could be very useful as an example FPGA configuration bit stream could be downloaded from a memory in parallel and faster with capacitive coupling approach than standard bus approach.

Still open problems have be address to be applicable this technology to a wide variety of commercial applications (heat, assembly of more than two layers, KGD and yield). A discussion is going to start with industrial partner to develop a full system prototype based on this technology.

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ARCES (University of Bologna) will continue research activities in the field of 3D computing architectures.
CEA-Leti intends to continue the development of this technology for future 3D devices and 3D system integration.
STMicroelectronics product division are investigating on potential benefits of this technology for future devices.

Project management and Coordination (WP5)

The project management has been carried out focusing on the following points:

- Management of the technical progress of the project
  - Periodic meetings have been held with variable frequency, according to the specific needs of the project. On average, we have met three times per year to assess the situation
  - Phone meetings have been held on a monthly basis to exchange information between designers and monitor the status of the project.
  - Interaction with the industrial partner. The input of the industrial partner has been carefully evaluated along the way and its suggestions coming from an expanding market perception of the relevance of this technology have been taken into account.
- Dissemination of the results
  - Publications at top international conferences have been achieved both concerning the design of the circuits and the development of the technology.
  - The technology developed in HighTree is conceived as a key ingredient for the development of new reconfigurable integrated systems that will be studied in an IP project submitted for evaluation in an IST call of the 6th framework.
- Protection of the Intellectual Property
  - Three patents have been filed by ST Microelectronics on inventions developed during this project.
- Training of researchers
  - Three Ph.D. positions have been activated to carry out the research involved in this project and we foresee the activation of three more positions in the next two years on the same subjects.

References and Publications

1] Mizoguchi et al. “1.2 Gb/s/pin wireless superconnect Based on Inductive Inter-chip Signaling”. ISSCC2004 pp.142-143 February 2004
2] Miura et al . “ A 1.95Gb/s 1.2W 3D-stacked Inductive Inter-chip wireless superconnect with Transmit power control scheme” ISSCC2005 pp 264-265 February 2005.
3] Kanda et al. “ 1.27Gb/s/pin 3mW/pin wireless superconnect interface scheme” ISSCC2003 pp 186-187 February 2003
4] Drost et al “Proximity Communication” IEEE J Solid State Circuits volume 39 Issue 9 pp 1529-1535 September 2004
5] Luo et al. “ 3Gp/s AC-coupled chip-to-chip communication using low-swing pulse receiver “ ISSCC2005 pp522-523 February 2005
6] Mick et al “ 4Gbps High density AC coupled Interconnection” CICC2002 pp133-140 May 2002

Papers accepted with results from High Tree

1) ***Electrical Measurement of alignment for 3D stacked chips***
R.Canegallo (STM), M.Mirandola, A.Fazzi.L.Magagni.R.Guerrieri (ARCES) K.Kaschlun(IZM-FHG)
ESSDERC- ESSCIRC 2005 will be presented in September

2) ***0.14mW/Gps High density capacitive interface for 3D system integration***
A.Fazzi, L/Magagni,M.Mirandola,R.Canegallo,S.Schmitz, R.Guerrieri
CICC2005 will be presented in September
3) ***Recent results on Advance molecular wafer bonding technology for 3D integration on Silicon***
Di Cioccio L, Biasse B, Charlet B, B, Kernevez N (CEA-Leti)
ECS Conference Quebec Canada.
4) ***3D Technology based on the wafer-to-wafer aligned direct bonding for capacitive coupling interconnectivity***
B. Charlet, L. Di Cioccio (CEA-LETI) , R. Canegallo (STM) , R.Guerrieri (ARCES UNIBO)
Submitted to AMC in September.

Patent pending in STMicroelectronics

1) ***Electrical measurement of alignment for 3D stacked chips***
2) ***Synchronous circuits for chip-to-chip communication***
3) ***Asynchronous circuits for chip to-chip communication***